DC Restored 100MHz Current Feedback Video Amplifier

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The EL2090 is an extremely versatile video amplifier with an integral on-board DC loop amplifier and sample-hold control circuitry. It is the first complete DC-restored monolithic video amplifier subsystem. It uses a current-feedback video amplifier with a nulling sample and hold amplifier specifically designed to stabilize video performance. This application note includes a video signal restorer with some fundamentals about DC restoration. As an application circuit of the EL2090, a x2 gain video amplifier is described together with a full evaluation circuit and double sided pc-board artwork. The EL2090 is a high-speed part, and some useful tips on layout have been included.

Although DC restoration is not a new concept, the high slew-rate, fast settling-time and low phase distortion at high frequencies provided by Elantec's family of monolithic current-feedback amplifiers, make CFAs the most attractive video amplifier choice for this application.

Video Signal Refresher

Figure 1 is a typical composite video signal which has a standard distribution level of 1V peak-to-peak into 75Ω, and comprises

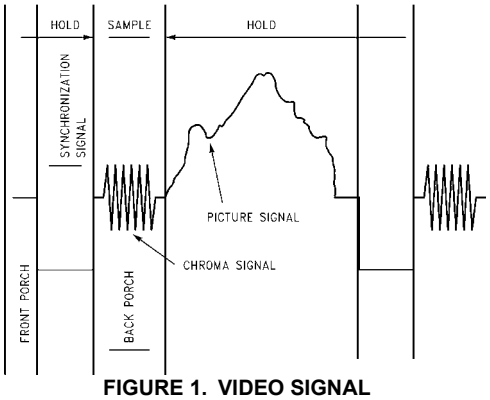

FIGURE 1. VIDEO SIGNAL

several sections. The video signal is the part containing the visible picture information, with a maximum amplitude between black and white of 0.7V. At the end of the picture information is the front-porch followed by a -0.3V of sync pulse, which is regenerated to provide system synchronization. The back porch is the part of the signal that represents the black or blanking level. In color NTSC systems the chroma or color burst signal is added to the back porch, normally occupying 9 cycles of 3.58MHz subcarrier (4.43MHz for PAL systems).

Video signals are often AC coupled to avoid DC bias interaction between different systems. The blanking level of the composite video signal needs to be restored to an externally set DC voltage, which locks the video signal to a predetermined common reference level, ensuring consistency in the picture displayed. This DC reference voltage V_R, sets and controls the picture brightness. The fundamental objective of the DC restore system is to force the DC baseline from the video amplifier to equal the externally set reference voltage V_R.

Figure 2 shows the schematic of a classical DC control servo system.

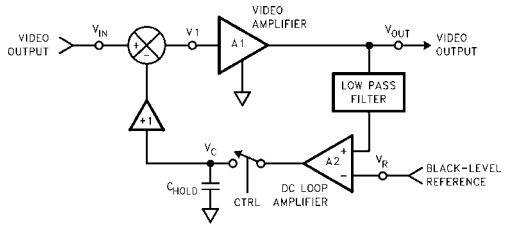

FIGURE 2. CLASSICAL DC CONTROL SERVO

The sync pulse is used to drive the control switch so that the DC servo loop is closed during the back porch of the video signal. The low pass filter removes the chroma burst. Operation of the DC loop is best understood by considering the voltage, V_C, across the hold capacitor, C_{HOLD}. During the back porch sample period, the switch is closed and the hold capacitor charges up. It can be shown from the loop dynamics that,

$$V_C = V_{BP} - V_{BP}/[A_1*A_2] - V_R/A_1$$

where V_{BP} is the average back porch voltage for the sample period.

The net result is that $V_{OUT} = V_R - V_{BP}/A_2$, which shows that the output is clamped to V_R with an offset term of $-V_{BP}/A_2$. This offset is clearly small with a high gain DC loop amplifier, A_2. The EL2090 has a DC loop amplifier gain of 15kV/V, reducing this offset to the order of a few millivolts. During the hold period the switch is open and the stored DC value of V_C is now subtracted from the incoming video signal, making

$$V_1 = V_{IN} - V_{BP} + V_R/A_1$$

and so

$$V_{OUT} = A_1 [V_{IN} - V_{BP}] + V_R$$

which effectively sets the back porch to V_R and the video signal is amplified by the forward amplifier with gain, A_1.

Subcircuits

The EL2090 DC restored amplifier is a 14-pin monolithic version of the circuit shown in Figure 2. The video amplifier,

A_1, is a 100MHz current feedback amplifier or CFA. These devices offer very high speed performance with excellent differential gain and phase. In many respects the CFA behaves as a conventional op-amp, but there are several key differences that must be considered by the user. In particular the two input impedances of the amplifier are different. The non-inverting input is high impedance and the inverting low impedance. However, the special feature of the CFA is that when in closed loop, the feedback current is determined by resistor, R_F, which controls the bandwidth of the amplifier independently of the gain setting resistor R_G.

The current feedback amplifier is essentially a transimpedance amplifier with an input voltage buffer to create a high input impedance non-inverting input. The transimpedance amplifier is formed by mirroring the output current of the input unity gain buffer into a high impedance internal Z-node and buffering this Z-node voltage through a low impedance output, as shown schematically in Figure 3 below.

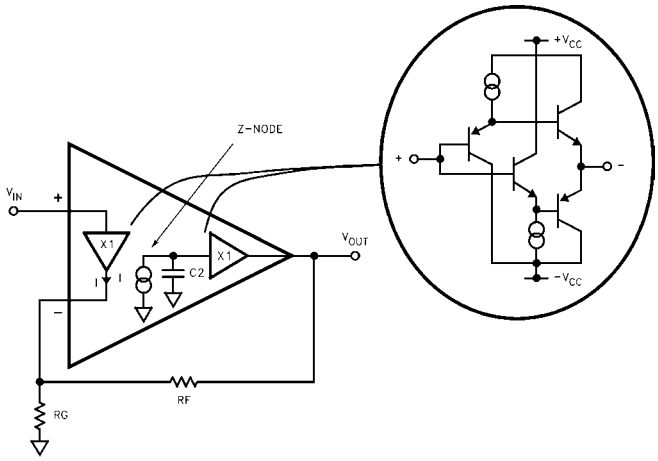

FIGURE 3. THE CURRENT-FEEDBACK AMPLIFIER

The unity gain buffers are a complementary class-AB common-collector stage, with DC current biasing. The slew-rate of the CFA is excellent due to the non-current-limiting input stage. The CFA has only one internal high impedance node (Z), so it is essentially a single pole dominant amplifier. Since the inverting input terminal is the output terminal of a voltage buffer, it is a low impedance point and the feedback signal is current. Intuitively one can see that in closed loop the feedback current through R_F supplies the current demanded by R_G and the input error current into the inverting input terminal. It is this feedback current component of R_F which is used to charge the compensation capacitance at the Z-node. Theoretically it can be shown that the -3dB bandwidth is approximately,

$$f - 3dB = 1/[2\pi R_F C_Z]$$

where C_Z is the compensation capacitance of the Z-node. However, as for conventional op-amps, the closed loop gain, A_1, is simply

$$A_1 = [1 + R_F/R_G],$$

and the -3dB frequency can be controlled with R_F while the closed loop gain can be set independently with R_G.

Features of the EL2090

Elantec pioneered the development of monolithic CFAs. A first to the market with the CFA the established reputation is confirmed with the EL2090 which is the first monolithic DC restored video amplifier. The device is built with Elantec's fast proprietary complementary bipolar technology which yields NPN and PNP transistors with equivalent AC and DC performance.

The on-chip current-feedback amplifier is optimized for video performance, and since it is a current-feedback amplifier it ensures that the -3dB bandwidth stays essentially constant for various closed-loop gains. The amplifier performs well at frequencies as high as 100MHz when driving 75Ω. The sample and hold circuit is optimized for fast sync pulse response; the switch operates in only 40ns. A particular feature of this sample and hold output buffer is its low output impedance which is fairly constant over frequency and load current. This provides good isolation and thus prevents the DC restore circuit from interfering with video amplifier performance through R_{AZ}.

Note that the burst output of Elantec's EL4581 and EL4583 sync separator chips can drive the Hold input of the 2090 directly.

Typical Application Circuit

Figure 4 shows a component level schematic diagram of the gain x2 DC restored video amplifier. The operation of the circuit is based upon the simple analysis given with the amplifier connected in the non-inverting mode of operation. The application circuit will restore the video DC level in ten scan lines, even if the hold pulse is as short as 2µs long. The current-feedback resistor R_F of 300Ω will give a stable bandwidth of 115MHz and all component values are chosen to maintain optimum speed and performance.

DC feedback resistor R_{AZ} is 2kΩ and is sufficiently larger than R_F to provide reasonable isolation between the sample and hold circuit and video amplifier and thus avoid any video signal coupling back to the sample-hold. R_{AZ} may be (optionally) split into two 1kΩ resistors and a 820pF bypass capacitor to reduce unwanted transient feedthrough from the sample and hold to the video signal to less than about 1mV seen at the amplifier's output. The circuit is designed to operate using ±15V supplies, but it can operate down to ±5V supplies by changing R_{AZ} and C_{AZ} values. Alternatively an inverting configuration video amplifier could be used with

appropriate exchange of the input signals to the DC loop amplifier.

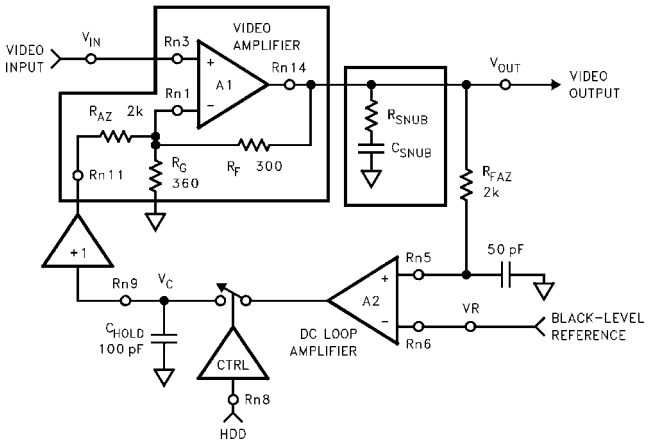

FIGURE 4. DC RESTORED VIDEO AMPLIFIER WITH $A_V = 2$

Design Procedures

1. Determining R_{AZ}

Ideally R_{AZ} should be large to provide good isolation between the sample and hold buffer and the video amplifier. This is because any video-induced current through R_{AZ} will cause changes in the buffer output impedance. A large series R_{AZ} will reduce the effect of buffer output impedance variations and thus preserve the differential gain error of the video amplifier. However, too large a value of R_{AZ} along with the output voltage compliance of the buffer will limit the maximum I_{AZ}, the DC correction current. A lower I_{AZ} will result in a lower restored reference level. Consequently, trade-offs have to be made between R_{AZ}, the maximum restored reference level, and the supply voltage which controls the output voltage compliance of the buffer. The following equations address some of the issues related to the trade-offs.

During the back-porch of the video signal, the sample and hold switch is closed. The servo loop charges C_{HOLD} to a voltage level necessary to bring the video amplifier output to the reference input level. The maximum voltage of C_{HOLD} is limited by the supply voltages.

$$V_{REF} = (V_{BP} * A_1) - V_{AZ} (R_F/R_{AZ}) \quad \text{(EQ. 1)}$$

where:

V_{REF} is the new stabilized back-porch level at the output of the video amplifier.

V_{BP} is the input back-porch offset voltage at the video amplifier input

A_1 is the close loop gain of the video amplifier.

$$A_1 = R_F (1/R_{AZ} + 1/R_G) + 1 \quad \text{(EQ. 2)}$$

R_F is the feedback resistor of the current-feedback video amplifier. It is nominally 300Ω for $A_1 = +2$. In gain of +5 application, R_F should be decreased to 270Ω to maintain gain flatness.

V_{AZ} is the buffered C_{HOLD} voltage developed by the loop to maintain the output at the reference level.

V_{AZ} is limited to the supply rails less 2.5V.

$$-V_{SUPPLY} + 2.5V < V_{AZ} < +V_{SUPPLY} - 2.5V \quad \text{(EQ. 3)}$$

Analysis of equation (1) shows that since V_{BP}, A_1, and R_F values are established by system requirements, the maximum R_{AZ} is determined by V_{AZ} and V_{REF}. A high R_{AZ} value requires a proportionally high V_{AZ} voltage and low V_{REF}. Outside the back-porch period, the switch is opened. The DC offset is maintained.

2. Design Example

Below examples are intended to show how R_{AZ} changes under different supply voltages and reference level.

Example A.

$V_{SUPPLY} = ±15V$

$V_{REF} = 0V$

$A_1 = 2$

$V_{BP} = ±1V$

$R_F = 300Ω$

Applying equation (3), the output voltage compliance V_{AZ} of the sample and hold buffer can be calculated,

$-12.5V \leq V_{AZ} \leq 12.5V$

Using equation (1), $R_{AZ} = 1.8kΩ$ for $V_{BP} = ±1V$.

Once R_{AZ} is determined, equation (2) gives $R_G = 360Ω$.

Example B.

$V_{SUPPLY} = ±5V$

$V_{REF} = 0V$

$A_1 = 2$

V_{BP} = ±1V

Applying equation (1), R_{AZ} = 375Ω for V_{BP} = ±1V.

Equation (2) gives R_G = 1.5kΩ.

Example C.

V_{SUPPLY} = ±15V

V_{REF} = 1

A_1 = 2

V_{BP} = ±1V

Applying equation (3),

-12.5V ≤ V_{AZ} ≤ 12.5V

R_F = 300Ω

Equation (1) gives

R_{AZ} = 1.2kΩ for V_{BP} = -1V

R_{AZ} = 3.75kΩ for V_{BP} = -1V

Therefore, R_{AZ} = 1.2kΩ

Using equation (2), R_G = 400Ω.

The above examples demonstrate the trade-off between the supply voltage, R_{AZ}, and the reference level. Examples A and B reveal that a lower supply voltage requires a lower R_{AZ}. Examples A and C show that when the supply rails are kept constant, a higher reference level requires a lower R_{AZ}.

3. Determine C_{HOLD}

Fast acquisition time is achieved with small values of C_{HOLD}, but this degrades droop performance. For video the droop needs to be better than 1/2 IRE in one horizontal line, or less than 3.5 mV in 45µs for NTSC. The droop is primarily caused by C_{HOLD} voltage decaying. Since the droop of C_{HOLD} is amplified to the output by the ratio R_F/R_{AZ} then C_{HOLD} must be chosen to satisfy dV_C/dt < 3.5 mV/45µs multiply R_{AZ}/R_F = 510 V/µs

R_F = 510V/µs.

Since dVC/dt = I_{DROOP}/C_{HOLD}, and the discharge current I_{DROOP} is a maximum of 50nA, then

C_{HOLD} • 98pF, or 100pF, the nearest preferred value.

If R_{AZ} is decreased for lower supply operation, C_{AZ} is correspondingly increased to preserve droop and acquisition characteristics.

4. Acquisition Time

Based on the values shown in Figure 4 the acquisition time is approximately 20µs. Note that it will take 10 chroma-burst of 2µs each to finish settling from a 1.0V input signal shift.

Evaluation Printed Circuit Board

- A component layout of the application circuit is shown in Figure 5(B) with some additional features.
- V_{REF} is applied externally to the grounded resistor R_{14}, which is decoupled with capacitor C_{11}.
- Optional 75Ω termination resistor has been included at the input and output.
- Built-in guard ring on PCB board layout [Figure 5(B)] ensures that leakage from the hold capacitor is minimal to improve droop performance. The guard ring is connected to the S/H Out. The hold capacitor should be low leakage and so mica or mylar capacitors are recommended here.
- Diode clamp circuit to overcome lock-up has been included on board.
- Optional AC input coupling capacitors of about 10µF has been included.
- Optional snubber circuit has been included.
- Optional R-C low pass filter on hold input logic drive has been included should the logic signal require slowing down.

Printed Circuit Board andLayout Hints

Figure 5(A)–(D) on following pages, shows a component layout together with double sided pc-board. Ground plane is essential throughout to reduce parasitic inductance and stray pickup. Special precautions have been taken to avoid any discontinuity in ground plane since this will make the function of ground plane much less effective. Supply decoupling capacitors are kept close to the power supply pins to ensure good power supply integrity. The feedback path of the video amplifier should be kept as small as possible to avoid deterioration in high frequency gain accuracy. BNC connectors are included at the input and output.

R1=360Ω
R2=300Ω
R3=1kΩ
R5=75Ω
R6=220Ω
R7=4.7kΩ
R8=10kΩ
R9=10kΩ
R10=2kΩ
R11=100Ω
R12=10kΩ
R13=75Ω
R14=10kΩ

C1=0.1µF
C2=0.1µF
C3=4.7µF (Tant.)
C5=820pF
C6=39pF
C7=50pF
C8=100pF
C9=0.1µF (Ceramic)
C10=4.7µF (Tant., 25V)
C11=4.7µF (Tant., 25V)
C12=30pF
C13=0.1µF (Ceramic)

POT1=10kΩ
D1=1N914
D2=ZN458B
D3=ZN458B (2.45 V_{REF})

FIGURE 5. COMPONENT VALUES

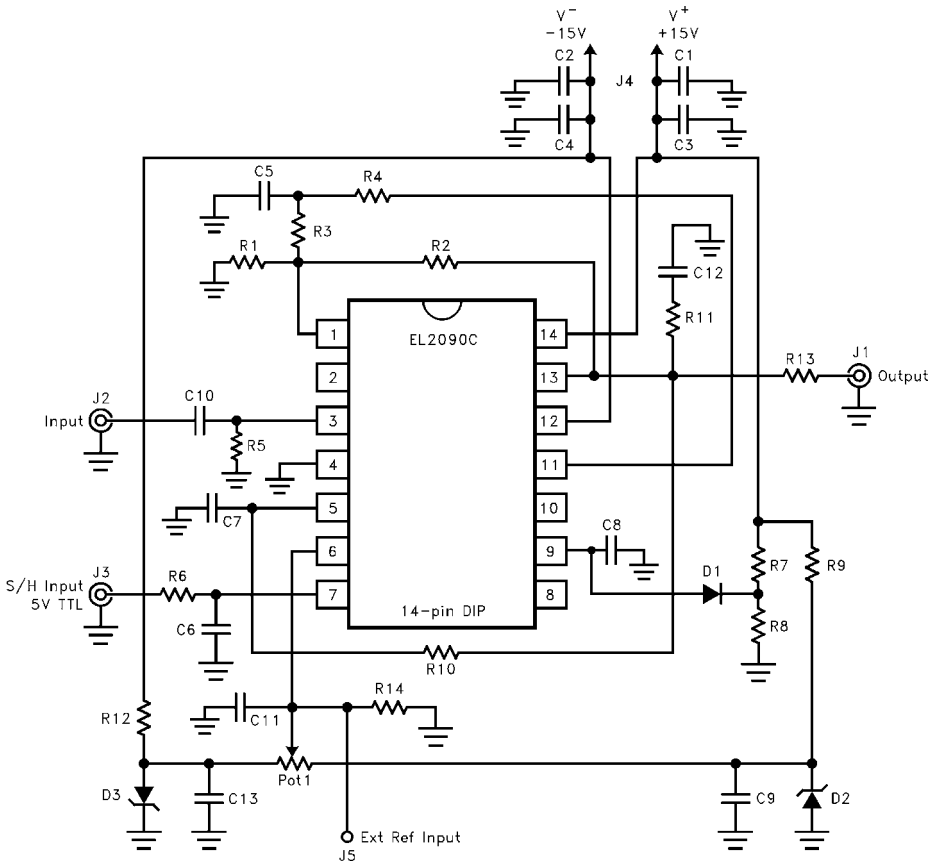

FIGURE 5A. SCHEMATIC

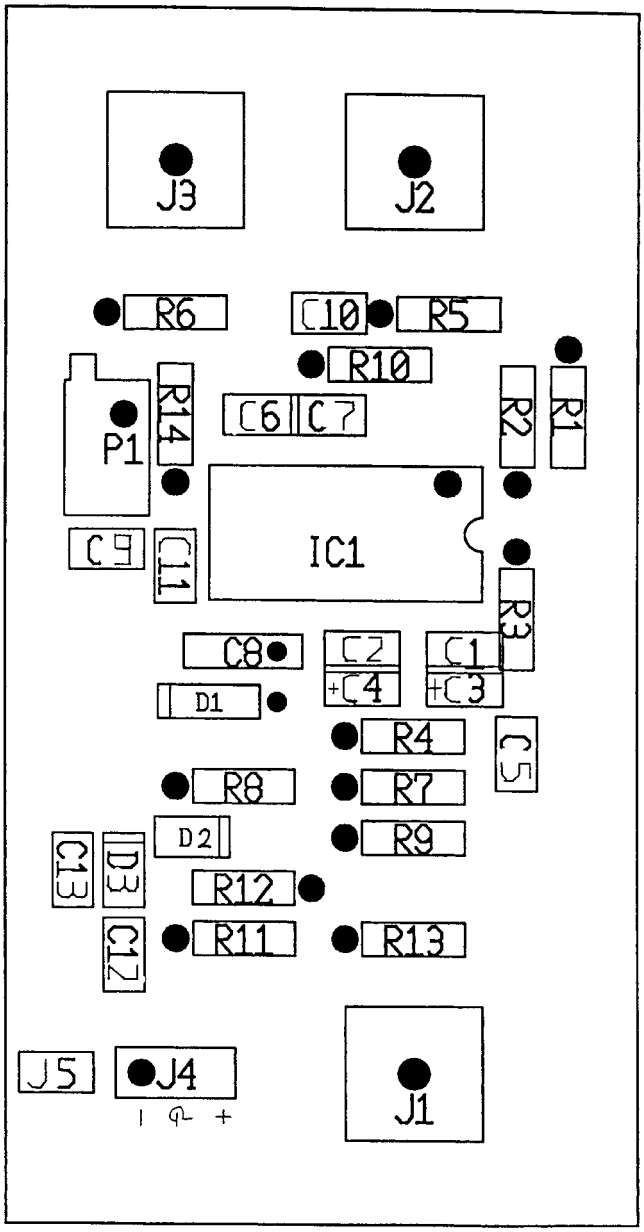
J3
J2
R6
C10
R5
R10
R14
P1
C6
C7
R2
R1
C9
C11
IC1
R3
C8
C2
C1
D1
+C4
+C3
R4
C5
R8
R7
D2
R9
C13
D3
R12
C17
R11
R13
J5
J4
J1

FIGURE 5B.

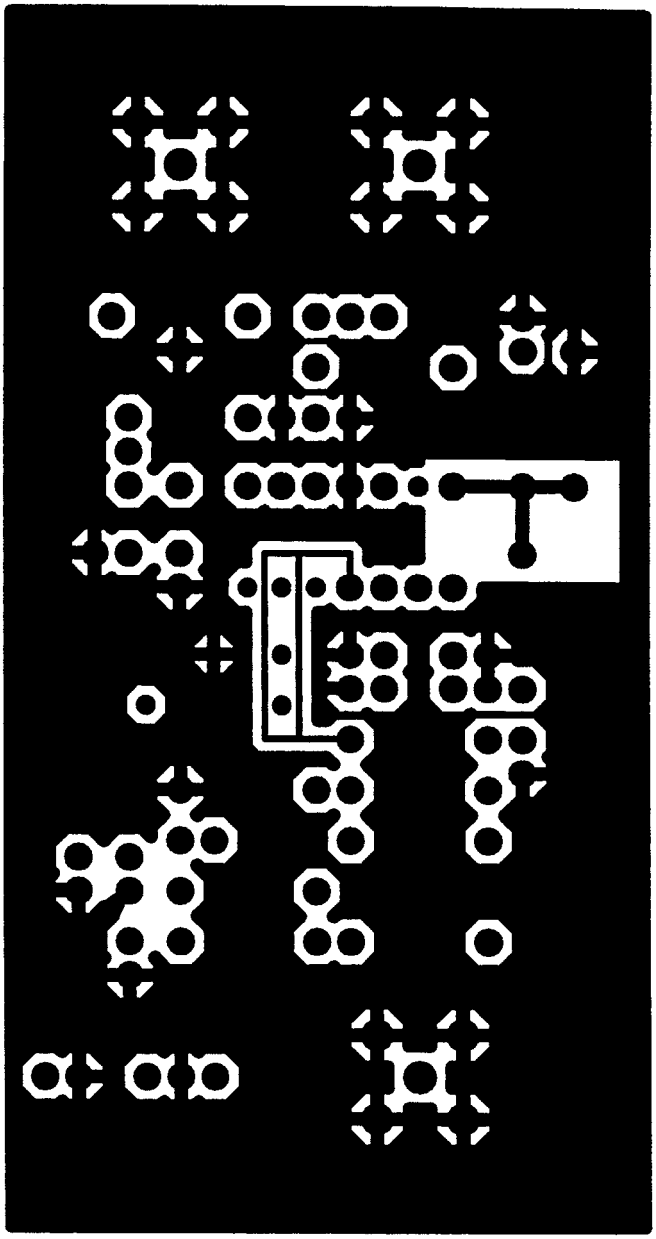

FIGURE 5C.

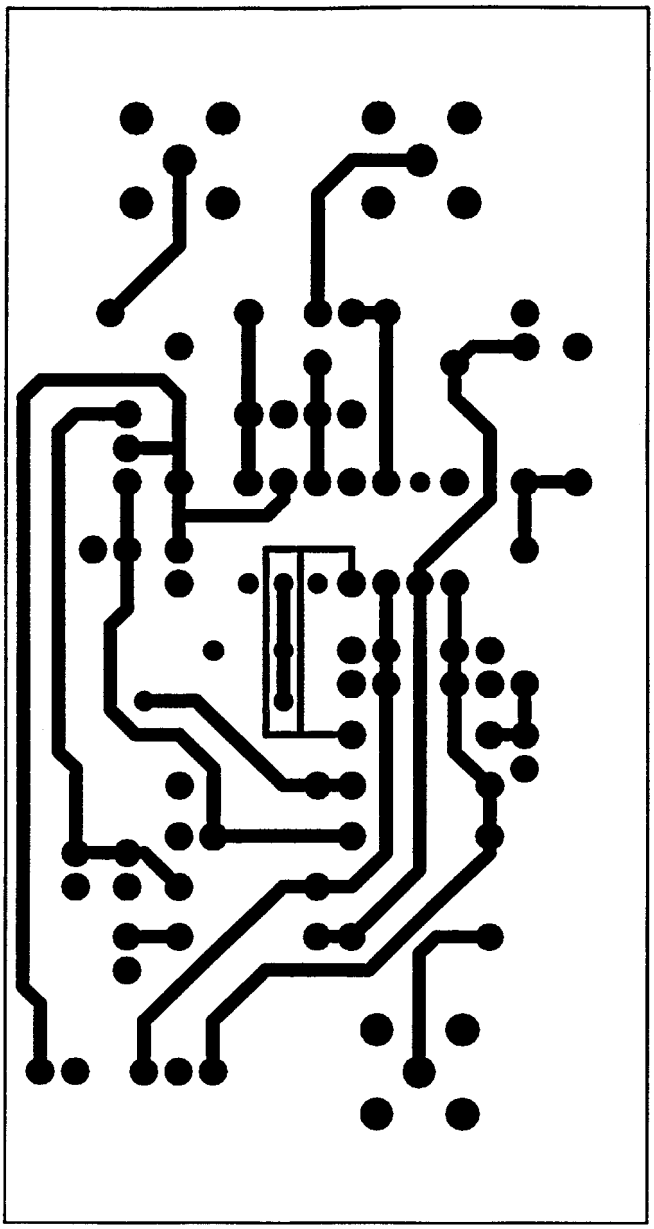

FIGURE 5D.

Do's and Don'ts

General Circuit Layout

As with all high frequency devices care must be taken with printed circuit board layout. Good ground plane construction is essential and DC power supply integrity must be ensured, so the power supply pins should be bypassed to ground with ceramic capacitors as close to the supply pins of the device as possible. The video current feedback amplifier is, like all CFAs, particularly sensitive to stray capacitance at the inverting input. This capacitance combined with the inverting node input resistance generates an additional high frequency pole in the feedback loop of the CFA leading to gain peaking in the response. Consequently pc-boards should be designed to keep lead lengths as short as possible around the inverting input node, with the ground plane positioned sufficiently far away to prevent this gain peaking effect.

Load Capacitance

In general load capacitance with negative feedback amplifiers causes gain peaking. This is because the load capacitance with the non-zero output resistance of the amplifier creates an additional pole in the feedback loop. The video CFA within the EL2090 is no exception to this and it may be necessary to add a series R-C snubber network to ground to minimize peaking, as shown in the data sheet, where the appropriate components are selected for a particular value of load capacitance.

Sample and Hold Section

Clock-feedthrough to C_{HOLD} leads to an undesirable hold-step, effecting the DC bias level.

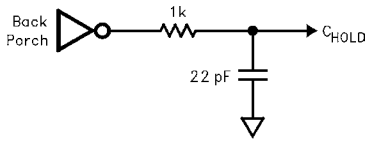

FIGURE 6.

Increasing C_{HOLD} is the most direct way of reducing this effect. Under normal operation the loop amplifier only deals with a small correction to V_C and although increasing C_{HOLD} will compromise the slew-rate of the sample-hold section, this is not a practical limitation. However with C_{HOLD} > 1 if and the sampling interval t_S < 2ms then on power up the device may lock-up if V_C approaches V_{CC}, causing the output transistors of the sample-hold amplifier to be taken out of their active region. The net result is that the lock-up does not self recover. Limiting V_C to V_{CC} - 3V using the external clamp circuit shown in Figure 7 prevents this lock-up condition from occurring.

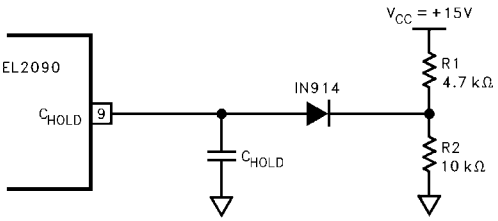

FIGURE 7.